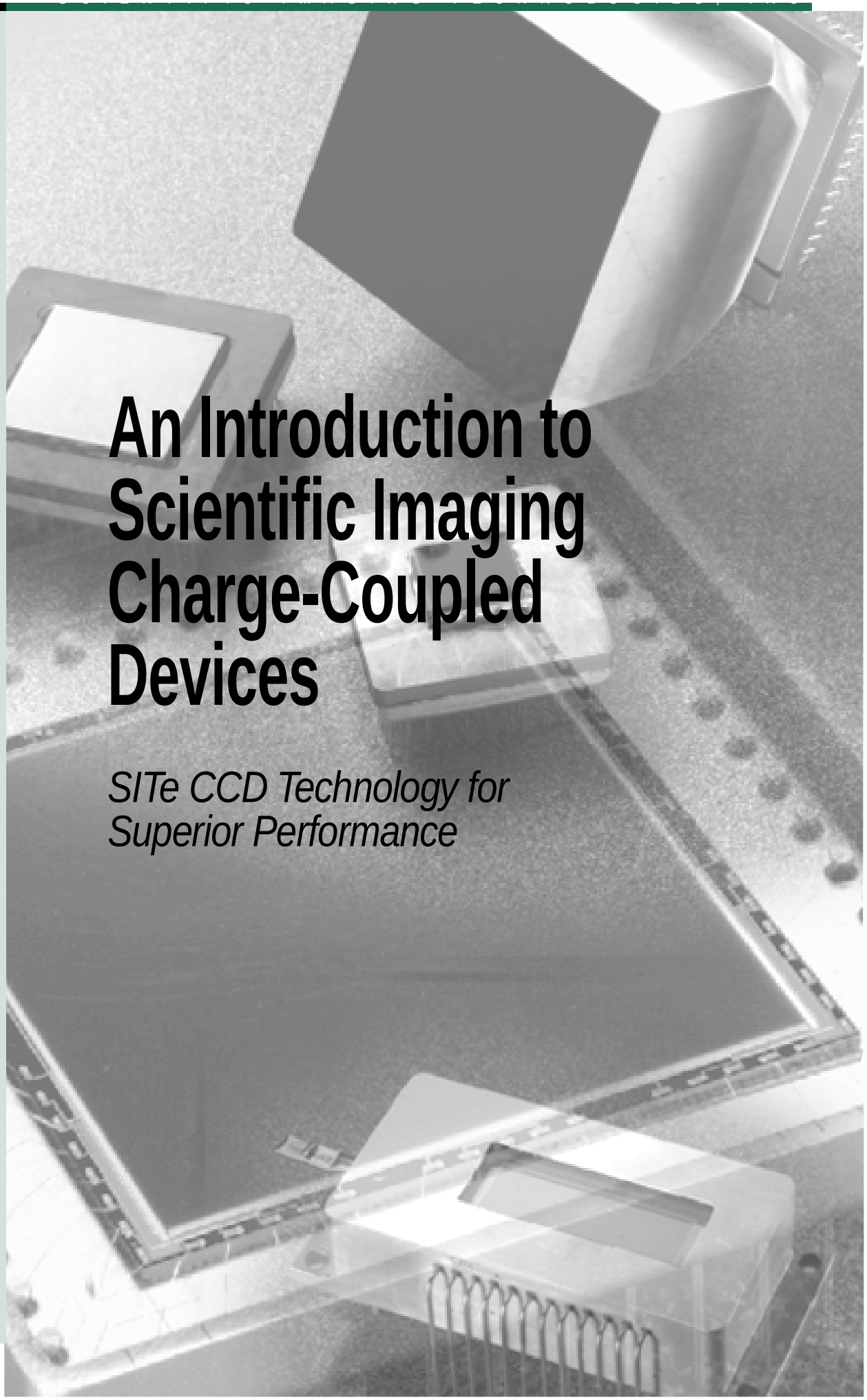

An Introduction to Scientific Imaging Charge-Coupled Devices

SITe CCD Technology for Superior Performance

ntroduction to the CCD

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Fundamentals

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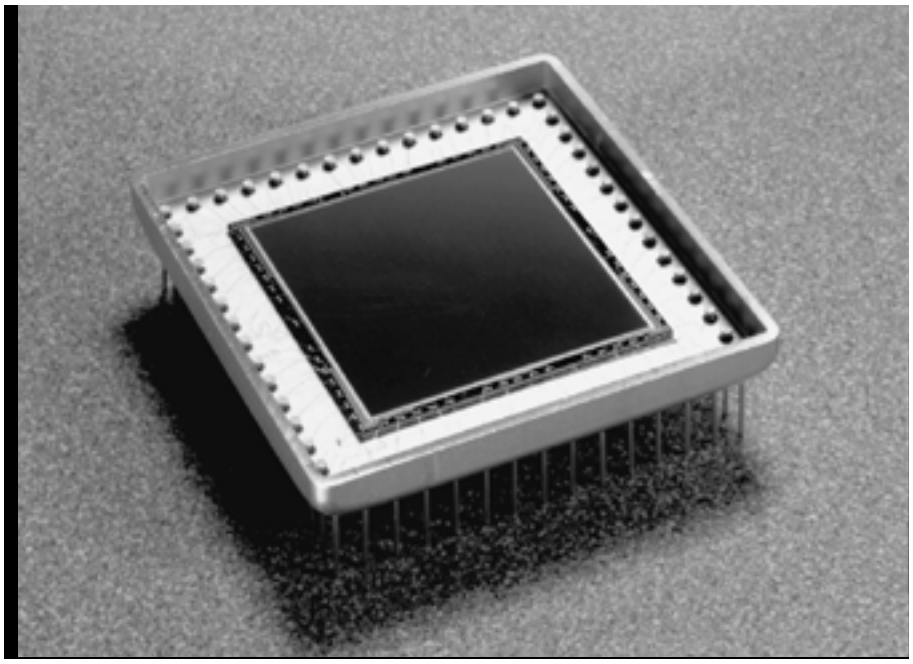

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Introduction

Charge-coupled devices (CCDs) are the key components in digital imaging cameras. CCDs take the place of vacuum tube-based imagers and film in conventional cameras. A high resolution camera can be constructed around this highly sensitive chip by combining it with a suitable lens system, a cooling method, and operating electronics. CCDs have wide application in a variety of scientific, astronomical, biomedical, and other commercial imaging areas.

With process development and design experience dating back to the founding of the group in 1974, Scientific Imaging Technologies, Inc. (SITe) has become an industry leader in the research, design, and manufacture of scientific-grade CCDs and imaging sub-assemblies which contain CCD components. SITe CCDs offer high quantum efficiency and sensitivity, high resolution, and a dynamic range that can exceed 100dB. SITe CCDs are sufficiently sensitive to detect reliably fewer than ten photons. Carefully designed and matched support circuitry enables SITe devices and systems to achieve optimum performance.

This technical note provides an introduction to the underlying concepts and operation of the charge-coupled device. SITe assumes that the reader has some understanding of basic solid state physics.

For more information about CCDs, contact the SITe customer service department.

Fundamentals

The MOS Capacitor

The simplest of all MOS (Metal-Oxide-Semiconductor) structures is the MOS capacitor. This device forms the basis for the charge-coupled device; an understanding of the structure is useful in order to comprehend CCD operation.

There are two types of MOS capacitors: surface channel and buried channel. These devices differ only slightly in their fabrication; however, the buried channel capacitor offers major advantages which make it the structure of choice for the fabrication of CCDs. Virtually all CCDs manufactured today utilize the buried channel structure, and we will focus on this preferred structure.

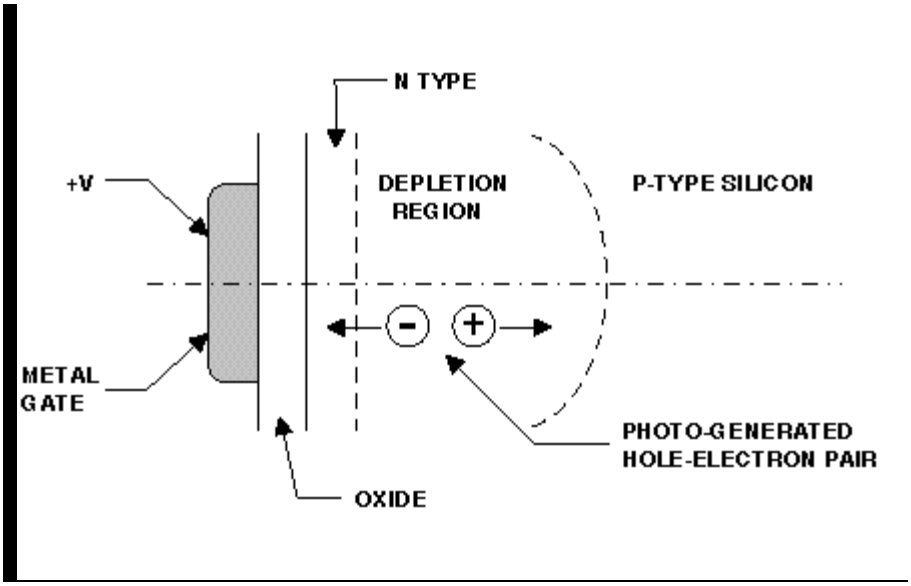

Figure 1
Buried channel capacitor.

Aschematic cross section of the buried channel capacitor is shown in Figure 1. Typically, the device is built on a p-type substrate, as shown. An n-type region (~1µm thick) is formed on the surface. Next, a thin silicon dioxide layer is grown (~0.1µm thick) followed by a metal or heavily doped polycrystalline silicon layer. The latter layer forms the electrode or gate and completes the capacitor.

Figures 2a, b, and c illustrate calculated electron energy and the electrostatic potential beneath the electrode for a typical buried channel capacitor at several different bias conditions. As usual, the electron seeks a condition of lowest potential energy. However, since the potential energy of the electron is

$$Ep = -|q|\Psi$$

electrons will seek a position where the local electrostatic potential is highest. (In this expression, q is the magnitude of the charge on an electron and Ψ is the electrostatic potential.)

For the unbiased condition (Figure 2a), the number of electrons in the n-type region is characterized by the equilibrium Fermi level. The bands are flat and the electrostatic potential is uniform within the n-type region. However, when the n-type region is fully depleted of electrons, a minimum occurs in the electron potential energy. The minimum is located within the n-type region and at some distance removed from the silicon-silicon dioxide ($Si\text{-}SiO_2$) interface (Figure 2b). This minimum in the energy (or maximum in the potential) is where excess electrons collect. (The difference between the buried and surface channel capacitors is the presence or absence of the n-type layer; in the surface channel structure, the potential maximum is located directly at the $Si\text{-}SiO_2$ interface.)

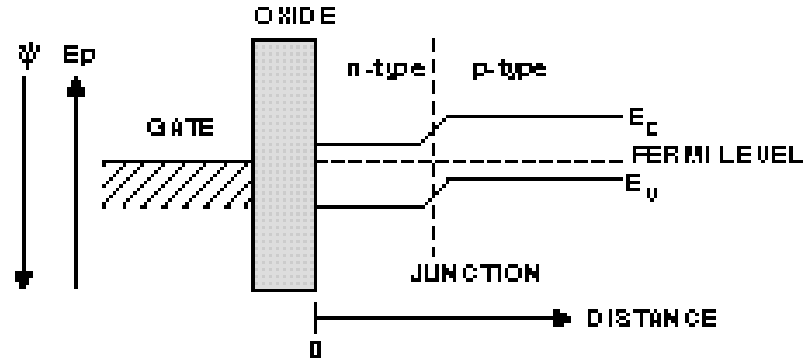

Figure 2A
Equilibrium energy band diagram.

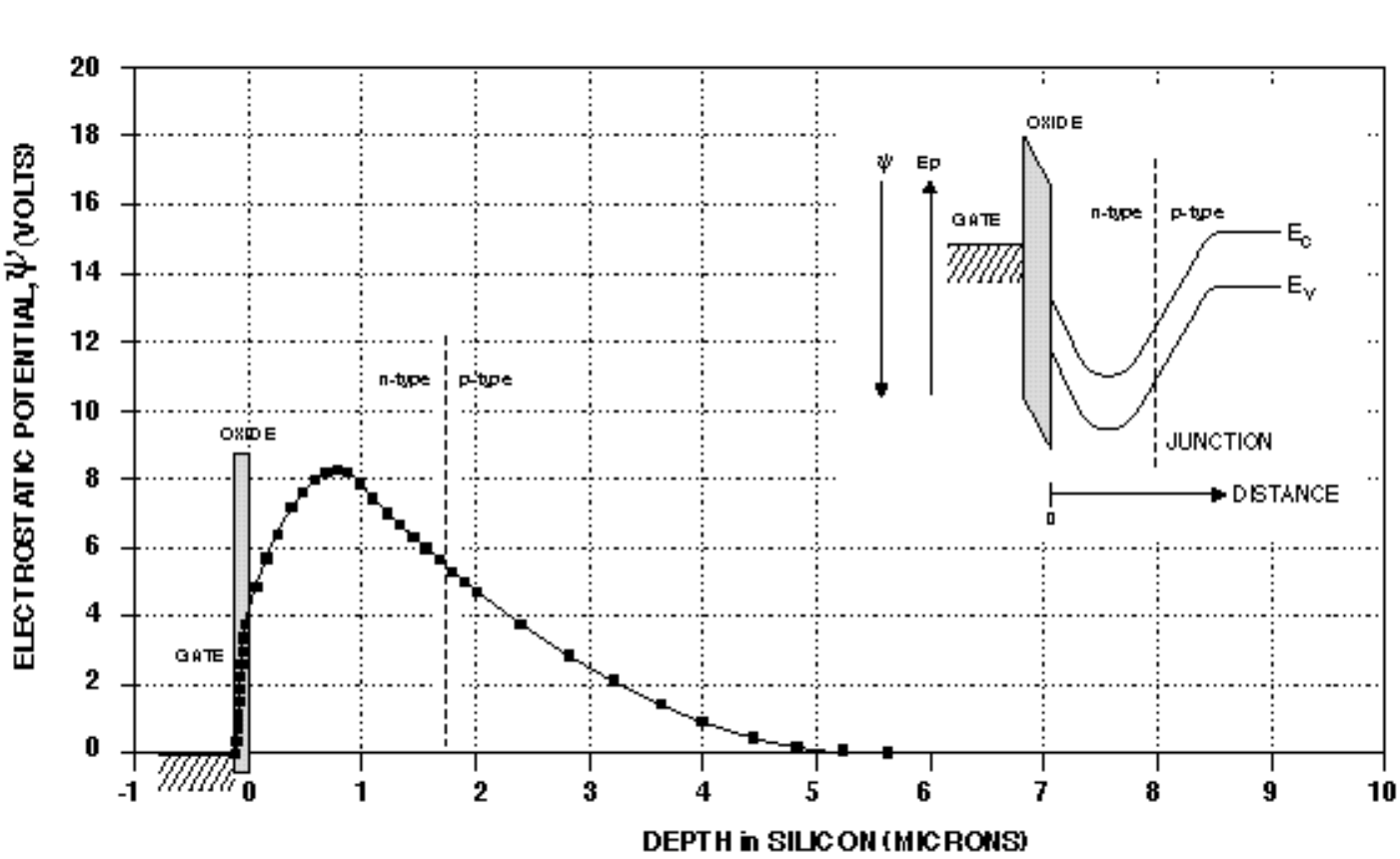

Figure 2B
Energy band diagram and electrostatic potential. Zero bias.

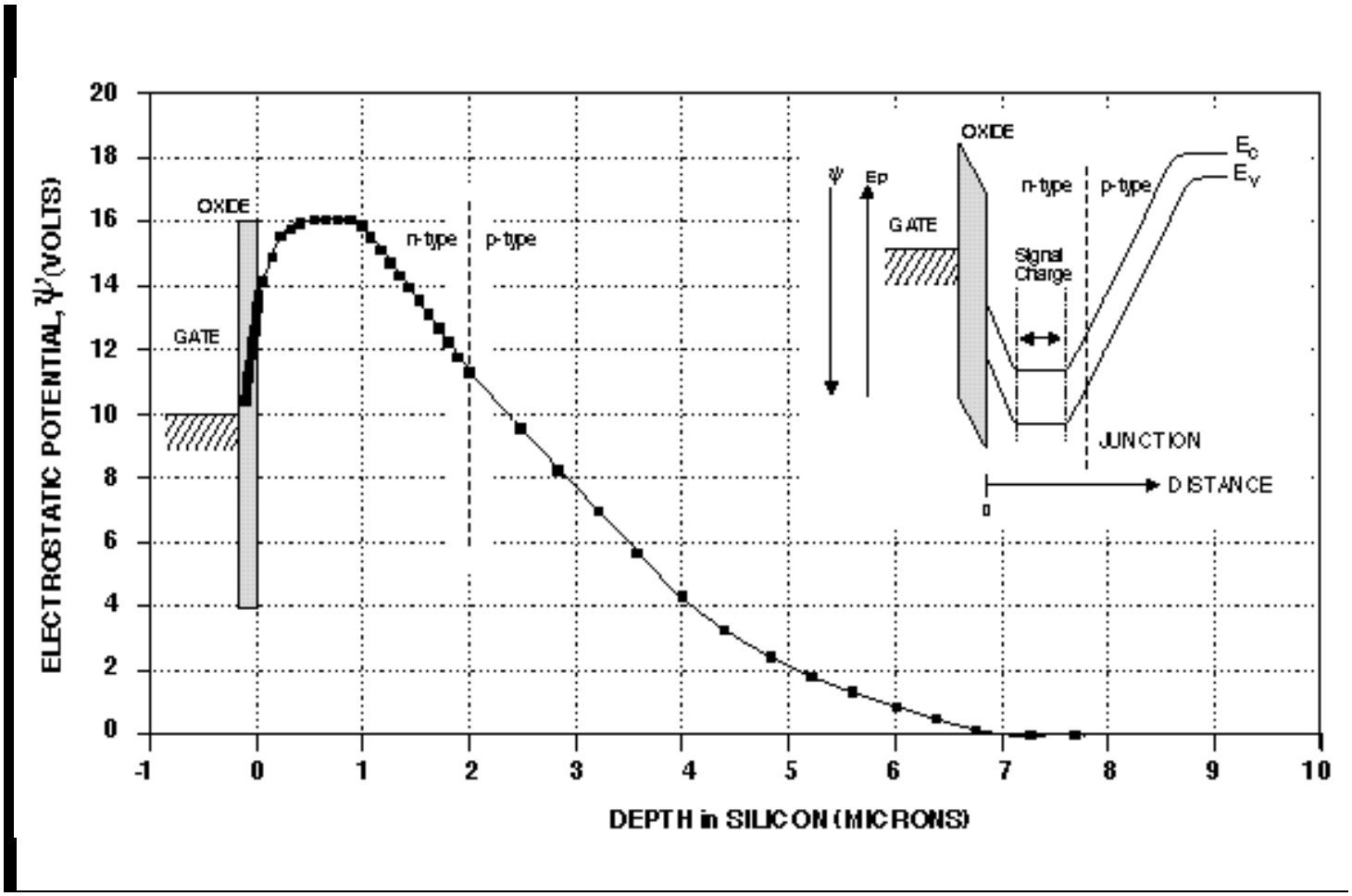

Figure 2C
Energy band diagram and electrostatic potential. 10 volt bias with charge.

Figure 2c illustrates the situation where a bias of +10 V has been applied to the electrode with the substrate held at ground potential and some charge (generated optically, for example) has collected in the potential minimum. The region where the charges collect is referred to as the channel; since this structure is below the silicon surface, the term buried channel is used. Note that the potential in the channel is flat (i.e. the field is zero) in the region where the charge has collected. If it were not, the electrons would move to make the field zero in the channel.

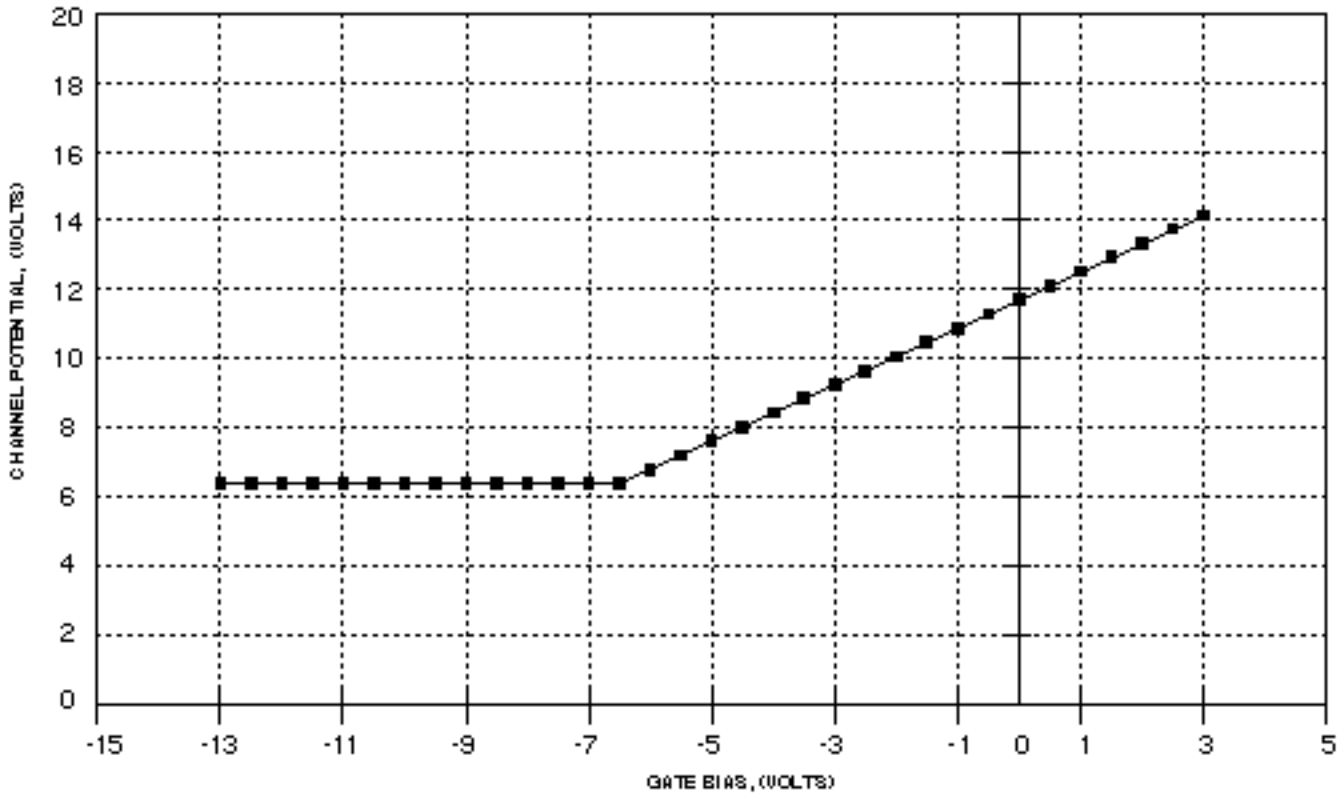

Figure 3
Typical channel potential as a function of gate bias.

The measured variation in channel potential, with the bias applied to the electrode, is illustrated in Figure 3 for a typical buried channel capacitor. Over much of the range of the gate voltage, the channel potential is essentially linearly related to the gate bias. However, for values of the electrode bias less than about -6 V the channel potential is pinned at a fixed value. This state is termed inversion. Under these conditions, the bias on the electrode is sufficiently negative to attract holes to the Si-SiO_2 interface. Any further decrease in the gate voltage merely attracts more holes to the surface and does not affect the underlying channel potential. This pinned feature of the channel potential curve is utilized in MPP operation which is discussed later. The exact form of the channel potential curve depends principally on doping concentrations, and the oxide thickness.

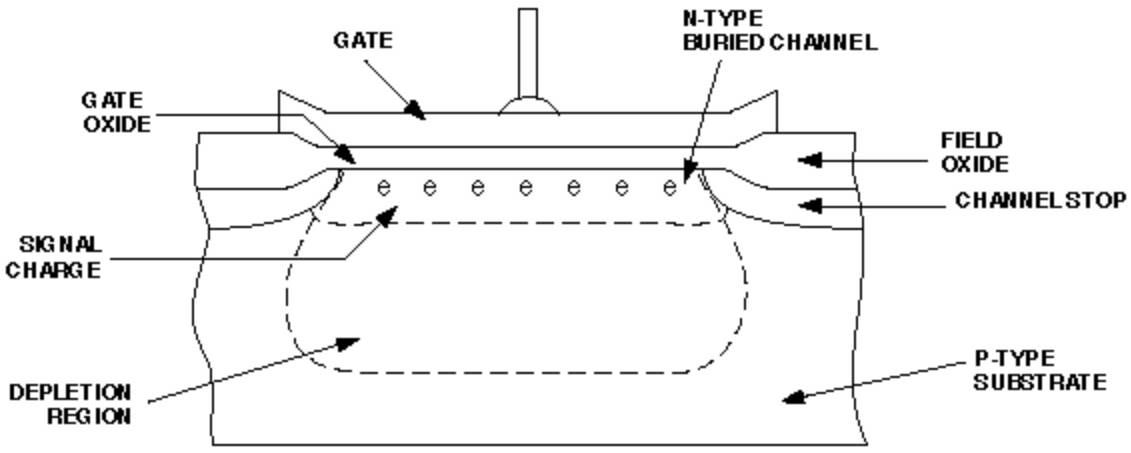

Figure 4
Practical buried channel capacitor.

Figure 4 illustrates a practical buried channel structure. The additional feature presented in this figure is the presence of field oxide regions on either side of the buried channel structure. These regions usually have heavily doped p-type diffusions beneath the oxide layer and because of the heavy doping combined with the thickness of the field oxide (~0.5-1.5µm), the electrostatic potential beneath the gate in this region is relatively insensitive to the voltage or changes in the voltage on the gate. In this way, charge which is collected in the buried channel device can be confined to a region beneath an electrode on top of thin gate oxide. These confining regions are called channel stops.

It is not necessary that the electrode be surrounded on all sides by field oxide. Note that the potential energy of an electron is lower under an electrode that is biased at +10 V than one that is biased at 0V. Consequently, a neighboring gate can also be used to confine the charge.

In summary, the features of the buried channel capacitor that make it attractive in scientific imaging applications are:

- the ability to create a potential well in a local region beneath a single electrode;
- the ability to modulate or control the potential under the gate;
- the storage location (channel minimum) is positioned away from the $Si\text{-}Si0_2$ interface and the states located there;
- low dark current makes it possible to store signal charge for long periods of time (tens of seconds to hours depending on operating conditions);
- the charge that collects can be generated optically, injected electrically, or created by charged particles such as cosmic rays, protons, or high energy photons (x-rays, gamma-rays);
- the ability to move charge from a position beneath one electrode to a second, neighboring electrode rapidly and with very low loss.

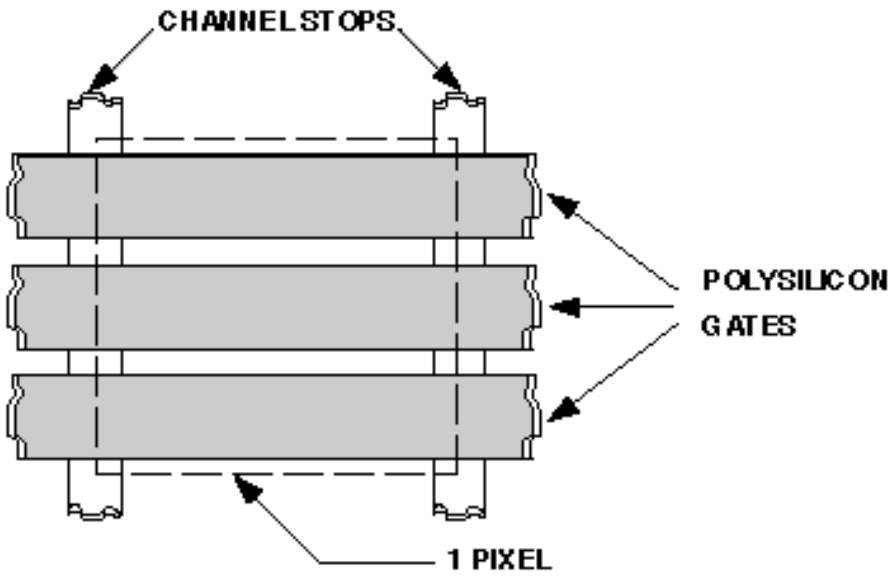

Figure 5
Three phase CCD pixel.

CCD Pixel

A single CCD pixel (picture element) is illustrated in Figure 5. This figure shows three polysilicon gates oriented perpendicular to two-channel stop regions. Between the channel stop regions lies the buried channel. If the potential on the middle electrode is more positive than that applied to either of the other two gates, a local potential energy minimum will be formed under the middle gate. When photons strike the pixel, electron-hole pairs are created via the photoelectric effect. Electrons created within the potential minimum will be collected there. Electrons that are created in the channel stop region or in the substrate beneath the pixel may diffuse to the minimum and be collected. In either case, the holes diffuse to and are collected in the p-type substrate. The quantity of charge that is collected in the well is linearly related to the intensity of the photon flux and to the time over which the light is allowed to fall on the pixel (integration time).

Other formats for the CCD pixel exist. There are structures that utilize two poly-silicon gates to define a pixel and some that use four. There is even a technology that uses a single gate in combination with multiple implants to define the pixel region. However, the technology most often used in the fabrication of scientific-grade CCDs is the three phase structure illustrated in Figure 5. The prevalence of the three phase technology is due principally to higher yield and process tolerance of this technology.

Dark Current

Dark current may be defined as the unwanted charge that accumulates in CCD pixels due to natural thermal processes that occur while the device operates at any temperature above absolute zero. At any temperature, electron-hole pairs are randomly generated and recombine within the silicon and at the silicon-silicon dioxide interface. Depending on where they are generated, some of these electrons will be collected in the CCD wells and masquerade as signal charges at the output. Large quantities of dark current limit the useful full well of the device, because the generation process is random, the dark current will contribute noise.

The principle sources for dark current in order of importance are generation at the silicon-silicon dioxide interface, electrons generated in the CCD depletion region, and electrons that diffuse to the CCD wells from the neutral bulk. The first two sources usually dominate the dark current. In addition, the generation rate can vary spatially over the array leading to a fixed pattern.

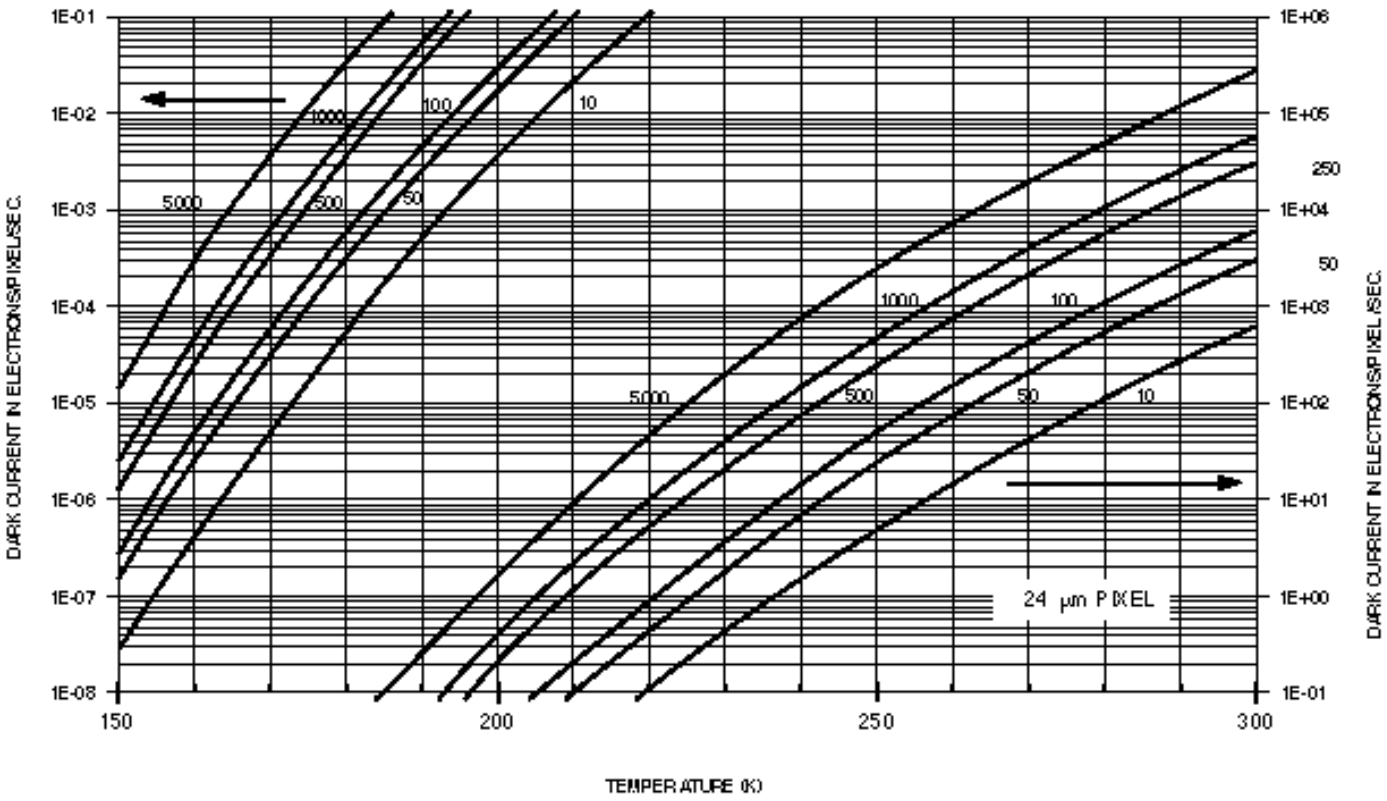

Figure 6
Effect of temperature on dark current e/pix/sec. Parameter is pA/cm² at 293K.

Fortunately, dark current sources are strongly temperature dependent. By sufficiently cooling the device, dark current can be effectively eliminated. The extent of cooling required depends largely on the longest integration time desired and the minimum acceptable signal-to-noise ratio. CCDs are most commonly cooled by using a liquid nitrogen dewar or by coupling the device to a Peltier cooler. The choice depends on how cold one must operate the device to achieve the desired performance.

Figure 6 presents calculations of the dark generation rate in e/pix/sec as a function of operating temperature for a 24µm² pixel. The parameter is the dark current in pA/cm² at a reference temperature of 293K. For example, if the system requirements dictate a dark generation rate of less than 0.0008 e/pix/sec. and one has a CCD that generates 10pA/cm² at 293K, the device must be cooled to -82° C. Conversely, if the requirements are such that cooling to -50°C is all that is practical and integration times are <1 second, then in order to ensure that, on average, the dark current contributes less than 10 electrons/pix/sec, any device with less than 500 pA/cm² dark current at 293K will suffice.

The curves in Figure 6 can be scaled for other pixel sizes simply by multiplying the dark current values by the ratio pixel area/(24µm)².

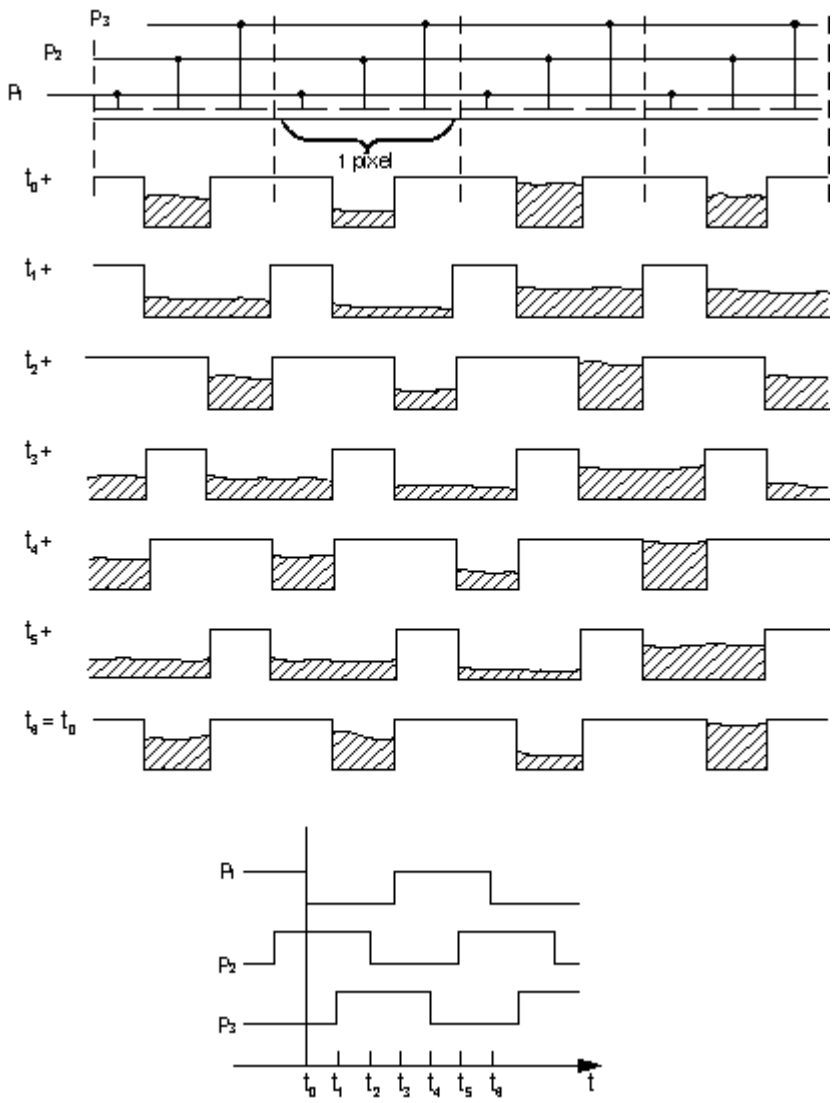

Figure 7
Three phase charge transfer process.

Charge Transfer Process

Acharge-coupled device consists of a regular array of individual pixels. Figure 7 illustrates a linear array of pixels, each with three separate gates, referred to as Phase 1, Phase 2, and Phase 3 (P1, P2, and P3). As shown within the linear register, all P1 gates are connected to the same bias or clock line; the same is true for P2 and P3.

Asingle CCD pixel (as defined above) has no means to read out the quantity of charge accumulated beneath the integrating electrode. The process of reading out this signal charge involves moving the packet from the site of collection to a charge detecting amplifier located at the end of the linear array. This is the charge transfer process, which is illustrated in Figure 7. Assume that charge is collected beneath the P2 electrodes. At time, t_1, we apply a positive bias to the P3 electrode equal to the P2 bias, turning the P3 electrodes "on". The charge located entirely beneath the P2 electrodes spills to the region beneath P3 due to self-induced drift and diffusion. At t_2, the P2 electrodes are turned "off" (i.e., the voltage applied to the P2 gates now equals that on the P1 gates). The charge under P2 now moves rapidly to a position beneath the P3 electrodes. Note that the charge moves from a position under the P2 gates to one under P3 gates. Indeed, the process of moving or coupling the charge from one gate to its immediate neighbor gives rise to the name charge-coupled device.

Repeating the process using the P3 and P1 gates results in the charge moving to a position under the P1 gates. One more cycle involving the P1 and P2 gates leaves the charge packet residing under the P2 gates again. Note that all charge

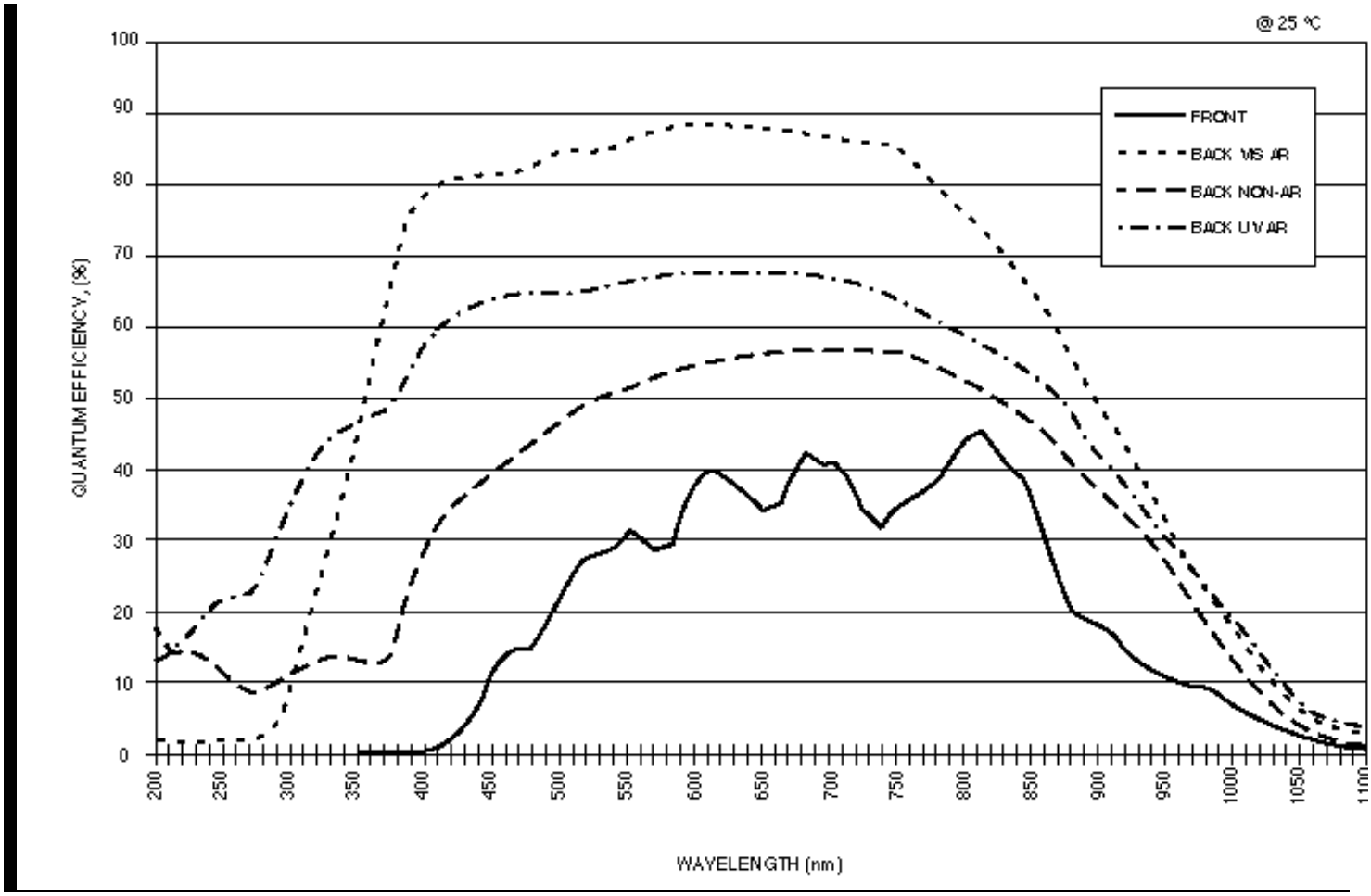

Figure 8
Typical quantum efficiency.

packets move simultaneously one pixel to the right. In addition, the first packet moves to the charge detection amplifier where the number of signal electrons is measured. N such clock cycles are required to readout an entire N-pixel linear register.

At all times within a single pixel, a well and a barrier to the next pixel co-exist. These are required in order to store the charge and to maintain the uniqueness and identity of each charge packet. Note that by interchanging the roles of any two of the gates the charge will move to the left. This flexibility is clearly another advantage of the three phase process.

The effectiveness with which the transfer process occurs is measured by the Charge Transfer Efficiency (CTE). Typically, charge may be transferred with an efficiency greater than 99.999% per pixel.

Quantum Efficiency

Quantum efficiency (QE) is the measure of the efficiency with which incident photons are detected. Some incident photons may not be absorbed due to reflection or may be absorbed where the electrons cannot be collected. The quantum efficiency is the ratio of the number of detected electrons divided by the product of the number of incident photons times the number of electrons each photon can be expected to generate. (Visible wavelength photons generate one electron-hole pair. More energetic photons generate one electron-hole pair per each 3.65 eV of energy.) The energy, E, of the incident photon in eV is

$$E = \frac{1.24}{\lambda}$$

where 1 is the photon wavelength in mm.

For wavelengths longer than about 300 µm, the number of collected electrons per pixel per second, Ne, is related to the

optical input power density, P, by the expression

$$Ne = 5.03 \cdot 10^{10} PA\lambda \cdot QE$$

where Pis the optical power density in µW/cm^2. A is the pixel area in cm^2, 1 is the wavelength in µm, and QE is the quantum efficiency in percent.

Front -Illuminated Devices

Figure 8 depicts the typical QE versus wavelength of various SITe CCDs. In the front illuminated mode of operation, incident photons must pass through a passivation layer as well as the gate structure in order to generate signal electrons. Photons will be absorbed in these layers and not contribute to the signal. Because of the high absorption coefficient for short wavelength photons in silicon, the quantum efficiency of front-illuminated CCDs is poor in the blue and UV regions. Interference effects in the thin gate structure cause undulations in the QE curve at the longer wavelengths.

Back-Illuminated Devices

In order to increase short wavelength quantum efficiency, SITe has developed a technique for thinning the silicon wafer to approximately 15µm and mounting the CCD with the gate structure against a rigid substrate. Light is incident on the exposed, thinned surface. The incident photons do not pass through the front surface electrodes and passivation layers. An enhancement layer is then added to the back surface to create an electric field that forces photo-generated electrons toward the potential wells under the gates. An anti-reflective (AR) coating may be added to increase optical quantum efficiency. Figure 8 shows QE versus wavelength for typical non-AR coated and AR coated SITe CCDs.

Enhancements

Multi-Phase Pinned Operation

Multi-phase pinned (MPP) devices have been developed to reduce or eliminate the Si-SIO_2 interface state contribuiton to dark current. As the gate electrode is driven to more and more negative voltages, a point is reached when holes are attracted to the interface. (See Figure 3.) Any further negative voltage merely attracts more holes. The presence of the high density holes at the silicon-silicon dioxide interface fills the interface states and reduces or eliminates this contribution to dark current. During integration, it is desirable to bias all the gates into inversion. However, in the normal CCD with all gates inverted, there is no barrier to separate pixel changes.

In the MPPdevice, an extra implant is placed under one of the electrodes (usually P3). The effect of this implant is to change the channel potential in such a way that when all the gates are biased into inversion, the channel potential beneath P3 still forms a barrier relative to the neighboring two gates. Charge collects under P1 and P2 while remaining separated from neighboring pixels.

In MPPoperation, it is possible to obtain dark current in the range of 10 to 50 pA/cm^2 and in some cases less than 10 pA/cm^2.

Mini-channel

The mini-channel is formed by placing an extra, low dose, n-type implant in the center of the buried channel of a CCD register. Its function is to increase the channel potential locally so that small signal packets (typically 4000 electrons) will be confined to the center of the channel. The advantage of the mini-channel is that it reduces low level signal interaction with defects in the channel. These defects would otherwise reduce the charge transfer efficiency. The addition of the mini-channel is particularly important for devices which operate in a radiation environment where protons and/or neutrons produce lattice damage in the CCD channel.

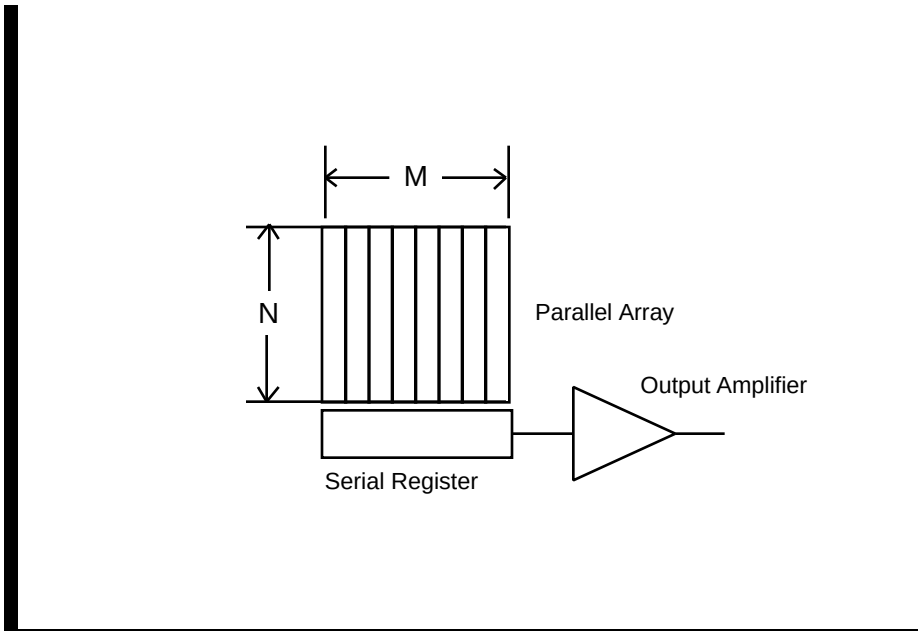

Figure 9
Imaging array.

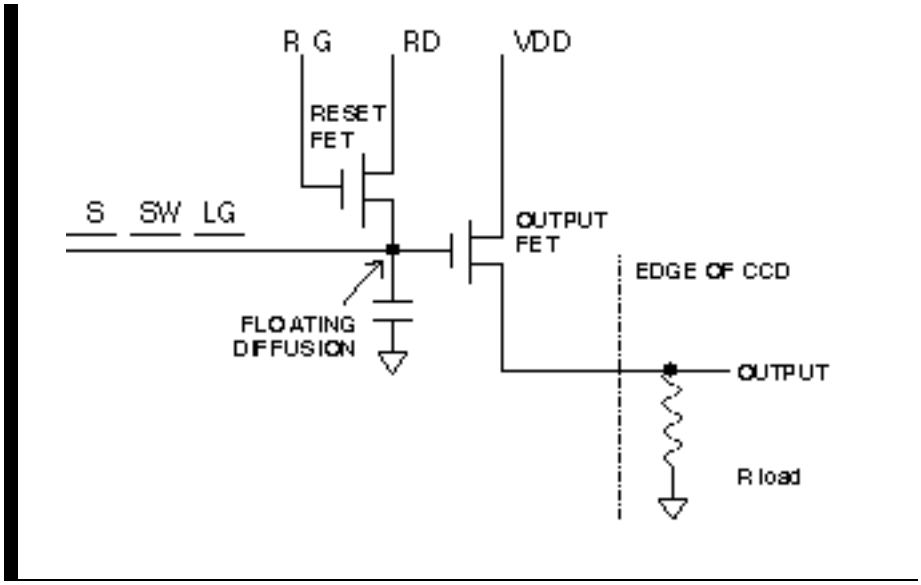

Figure 10
Floating diffusion output structure.

The CCD Imaging Array

Imaging Array Basics

Imaging arrays usually consist of square or rectangular arrays of pixels. An M x N array may be thought of as a collection of M linear registers of N pixels each. The M linear registers are aligned vertically side by side and separated by channel stop regions (see Figure 9).

An additional independent linear register is placed next to the array with its charge transfer direction orthogonal to that in the array. This serial register is arranged so that there is a single pixel adjacent to each of the M columns, and is terminated in a charge detection output amplifier.

Following an integration period, array readout involves simultaneously clocking all rows of charge packets one pixel toward the serial register. This transfer process causes the bottom row to transfer into the serial register. The charge packets are then transferred along the serial register toward the output amplifier where they are detected. The resulting data stream is a pixel-by-pixel, row-by-row representation of the image falling on the CCD.

Output Structure

At the end of the serial register is an output amplifier that converts electronic charge to a voltage. Atypical output structure is shown schematically in Figure 10.

The output structure consists of two buried channel MOSFETs and a last gate. The function of the last gate is to isolate the floating diffusion from the serial clocks. The last gate has a separate lead and is generally provided a DC bias somewhat more positive than the low rail of the serial gates. The source of the reset FET lies adjacent to the last gate. This n^{+}-p diode can be modeled as a capacitor between the channel and the substrate. This diffusion is also connected to the gate of the output FET. When the reset FETis of f, this diffusion is electrically isolated and is referred to as the floating diffusion or the output node. The total capacitance of the output node, C_T, is the capacitance of the floating diffusion plus the parasitic capacitances associated with metal leads and the gate of the output FET.

Reading out a pixel begins by turning on the reset FETand setting the floating diffusion to the reset drain voltage. The

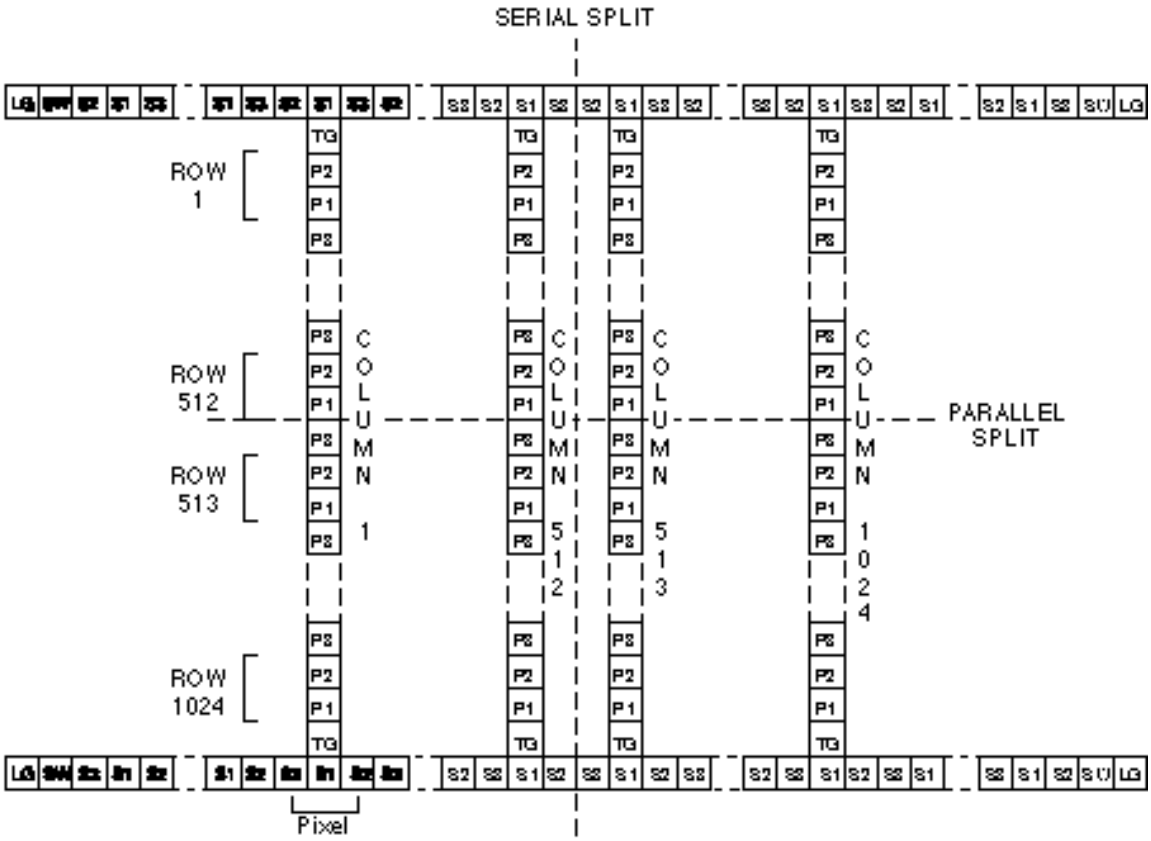

Figure 11
Functional diagram.

reset FETis then shut of f, isolating the floating diffusion. When the final serial gate voltage is dropped, (Figure 10) any electrons stored under the gate pass under the last gate and onto the floating diffusion. The change in voltage at the output, ΔV, is directly related to the quantity of charge, ΔQ, that is transferred to the floating diffusion and the gain G at the output FET

$$\Delta V = \frac{\Delta Q}{C_T} G$$

The charge of one electron on the floating diffusion capacitance is enough to change the output voltage by about a microvolt. The floating diffusion charge versus output voltage relationship is generally linear over many decades. The slope of the curve (in microvolts per electron) is referred to as the output sensitivity or conversion gain.

Although the output signal is actually voltage, it is common practice to refer to the CCD output signal in terms of electronics.

Many SITe CCDs incorporate a lightly doped drain (LDD), a fabrication technique designed to reduce the overall capacitance of the output sense node. The effect is to increase the conversion gain of the output amplifier and reduce the noise.

The Functional Diagram

The functional diagram is a schematic representation of the CCD in which each gate is represented by a box so that appropriate clocking may be determined. Figure 11 uses a SITe 1024 x 1024 CCD array as an example. The imaging area consists of 1024 columns isolated from each other by the channel stop regions. Each column contains 1024 pixels defined by the polysilicon gate structure. The three phases of the parallel gate structure are represented by P1, P2 and P3. The parallel array is divided into halves, top and bottom. In each half, all the P1 gates are connected together. The P2 and P3 gates are similarly connected. Serial registers are located at the top and bottom of the array perpendicular to the channels in the parallel array. The serial registers are also separated into halves, left and right. The gates in these registers are represented by S1, S2 and S3. In each half, all the S1 gates are connected together, all S2 gates and all S3 gates are connected in a similar fashion.

The parallel array is coupled to the serial registers through a transfer gate (TG in the diagram). This is a separate parallel gate which is driven to a high state during transfer of a line into the serial register, then switched to a low state while charge is being moved along the serial register. The transfer gate also isolates an unused serial register preventing unwanted charge from entering the array.

The serial registers extend beyond the parallel array. These extra pixels provide a reference signal for calibration, since they do not receive charge directly from the parallel register. At each end of the serial registers there is a summing well (SW) adjacent to the last gate (LG). The summing well is similar to the other serial gates but is connected separately. It's function is to provide a means to sum consecutive charge packets in the register without adding noise in the process. An output amplifier is located at each end of each serial register. Thus, there are four outputs available for readout.

This example CCD imager may be read out with one, two, or four outputs operating simultaneously. When operated in the full frame mode, the entire image is transferred to one output, and all of the same numbered phases are clocked together. The charge may be clocked out of any output, however; the timing must be appropriate for that output. The gates of the unused serial register can be clocked or held at a dc level.

The CCD may also be operated in four output (quad) mode wherein charge is clocked to all four outputs simultaneously. The charge in each quadrant is transferred to the amplifier closest to it. The gates in each quadrant are driven as appropriate for full frame operation of that output.

Finally, the CCD illustrated in Figure 11 may be operated using two outputs simultaneously. Timing for each of the halves much be appropriate for the selected outputs. To read out through two amplifiers on the same serial register, the serial gates are driven as in the quad mode while the parallel array is operated in the full-frame mode. Conversely, to read out through the amplifiers on opposite serial registers, the parallel array is operated as in quad mode, and the serial registers are clocked to transfer the charge to the selected amplifier. This again illustrates the flexibility of the three phase process.

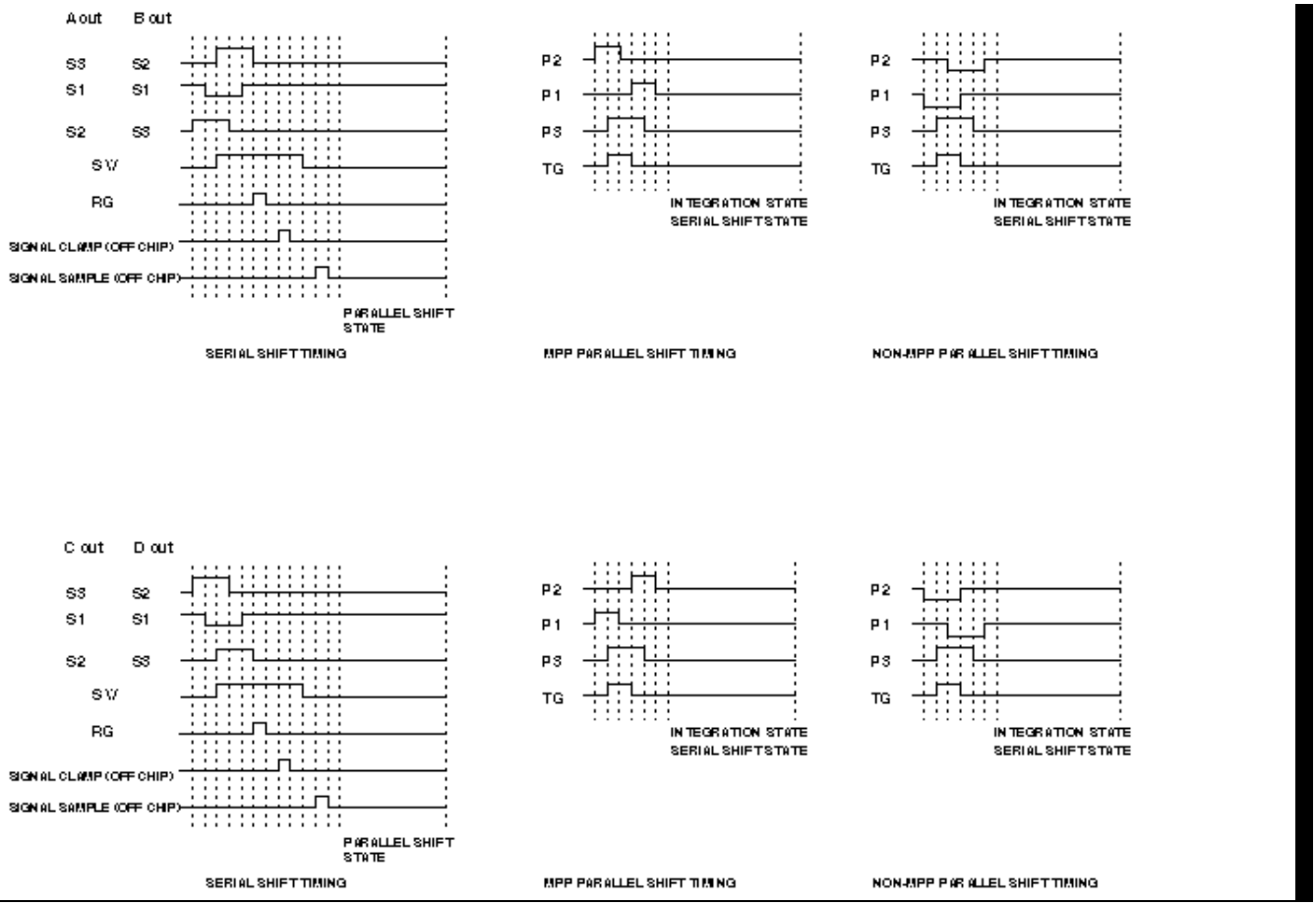

Figure 12
Typical CCD timing.

The Timing Diagram

Figure 12 details a typical CCD timing sequence. The parallel shift timing sequence is repeated once per row of pixels transferred to the serial register. Then the serial shift timing is repeated sufficiently to transfer all of the pixels in the serial register to the output.

Several rules apply in generating the serial and parallel timing. In order to preserve the identity of change in each pixel, all gates may not be high at the same time, and for non-MPP devices, all gates must not be low at the same time or else charge from adjacent pixels will diffuse together. As discussed earlier, MPP devices have a built-in potential barrier under one gate, so all parallel gates may be low during integration. Also, to preserve charge integrity, the MPP barrier phase must not be the last to drop nor the first to rise.

Two adjacent gates may not fall at the same time or charge transfer efficiency will suffer. For example, when transferring charge from the parallel array to the serial register, the last parallel gate must fall, followed by the transfer gate; then the serial transfer may commence. The last parallel gate and the transfer gate must not fall together.

A gate transition is started at the beginning of a state and is assumed to have changed to the other level by the end of the state. Each state must be long enough for the gate voltage to have changed for all parts of the array. Particularly in the parallel array, each pixel has a capacitance and is separated from its neighbors by resistance. The transitions of the gates in the center of the array will not be completed until some time after the voltage at the package pin has reached its final value.

From the functional diagram, it may be seen that there are a number of pixels between the edge of the parallel array and the output. These “lead in” pixels will be empty at the beginning of each row. If more serial pixel shifts are made than the sum of the lead-in pixels and the number of columns In the parallel array, these overscan pixels will also be empty. These trailing pixels contain very little dark current so that their level and noise content represent a reference dark level and system plus imager readout noise.

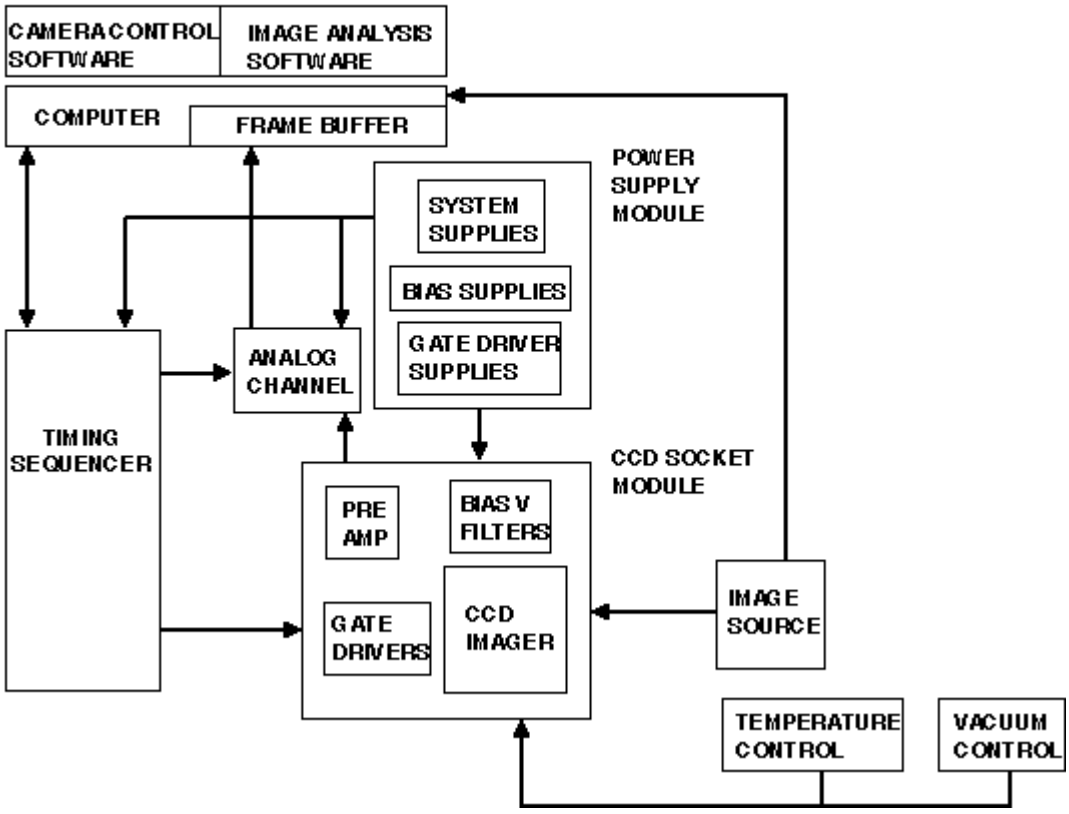

Figure 13
Typical CCD electronics.

Support Electronics

Architecture

The architecture of typical CCD support electronics is shown in Figure 13. It consists of modules commonly found in scientific-grade CCD cameras.

At the center of the diagram is the CCD module containing the CCD imager, gate drivers, output signal preamplifier, and the low pass filters for the bias voltages. This module is supported by the modules around it. CCD operation is controlled through the logic signals which are outputs of the timing sequencer. The timing sequencer coordinates the time critical tasks associated with reading out and digitizing an image.

Signal Processing

Anumber of methods have been developed to measure small changes in output voltage and minimize the contribution of noise sources both on and off chip. The largest source of on-chip noise is the so-called reset or KTC noise. It is manifested as an uncertainty in the floating diffusion voltage after the reset FET has turned off and may be hundreds of microvolts in amplitude. It arises from the thermal noise of the non-zero resistance of the reset F E T. After the reset FET is shut off, howev- e r, the floating diffusion voltage remains constant. Reset noise may be eliminated by taking the difference between the output voltage level sampled after reset and again after the summing well has dropped and transferred signal charge to the floating diffusion. This method of sampling the voltage twice is known as correlated double sampling (CDS). All but the highest speed CCD signal processing electronics use this method.

There are two sources of noise in the output amplifier itself. First is the thermal (white) noise caused by the parallel resistance of the output FET and the load resistor. Second is the 1/f or flicker noise associated with the surface states in the

output FETgate region. Thermal noise can be reduced by limiting the bandwidth and increasing the sampling time; however, at some low bandwidths, 1/f noise will dominate the total noise.

CCD signal processing electronics generally consist of a pre-amplifier, a bandpass filter, a circuit that accomplishes correlated double sampling, and an analog to digital converter (ADC). For practical purposes, the signal must be AC coupled at the CCD output, DC restored at some point, inverted, and amplified to match the range of the ADC.

There are many methods of implementing correlated double sampling depending on the desired pixel rate. Two common methods discussed here are the dual slope integrator and the clamp/sample amplifier.

The dual slope integrator is a slow speed (<500 kpixels/sec), low noise approach often used with 16 bit ADCs. As shown schematically in Figure 14, the circuit involves an integrating amplifier and a means to invert the input signal.

At the beginning of the readout sequence, the integrating capacitor is shorted to discharge it and remains shorted through the CCD reset period. When the output voltage has settled, the shorting switch is opened and the inverted output level (with no signal present) is integrated for some time. As the summing well's charge is transferred onto the floating diffusion, the input is switched to the non-inverted signal and integrated for the same amount of time. Then the output signal is sampled by the ADC. This circuit has the advantage of providing high frequency filtering and gain; however, its speed is limited.

For higher speeds, the clamp/sample circuit is often used. As shown schematically in Figure 15, the circuit consists of a storage capacitor, a switch, and an inverting gain amplifier.

The clamp switch is closed at the beginning of the readout sequence and remains closed through the CCD reset period. When the output voltage has settled, the switch is opened and the input of the amplifier is allowed to change. After the summing well has transferred its charge onto the floating diffusion and the signal has risen, the output may be sampled. An inverting gain amplifier is needed to provide the gain and inversion

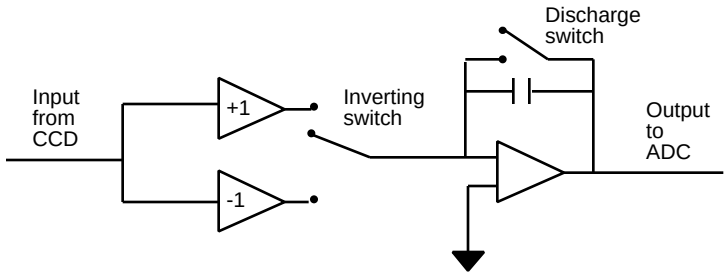

Figure 14
Dual slope integrator.

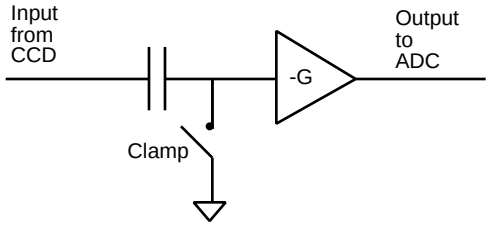

Figure 15
Clamp/sample amplifier.

present in the dual slope integrator.

The CCD output noise is on the order of a few microvolts. Thus, the choice for preamplifier is critical to obtain optimum noise performance. To this end, it is important to select a preamplifier that is matched to the bandwidth of the system and has the lowest possible current and voltage noise.

Gate Drivers

Gate drivers are essentially switches between two voltage levels. Several characteristics are desirable. First, the logic level input is usually ground referenced and needs to be isolated from gate voltage levels. The permissible output transition rate is limited by the gate capacitance and gate resistance. Too rapid a transition will adversely affect adjacent gates by reducing full well capacity on negative transitions or by driving the charge into the Si-$Si0_2$ interface on positive transitions. The gate drivers should also have sufficiently low output impedance to sink the current that flows when adjacent gates are driven.

In summary, support electronics must be carefully designed to obtain the best possible performance from scientific-grade CCDs.

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SITe Specifics

Scientific Imaging Technologies, Inc. (SITe) specializes in the research, design, and manufacture of charge-coupled devices (CCDs) and imaging subassemblies containing CCD components. SITe's scientific-grade CCDs are used in applications for astronomy, aerospace, medical, military surveillance, spectroscopy, and other areas of imaging research. Commercial uses of SITe high performance CCDs include biomedical imaging, manufacturing quality control, environmental monitoring, and non destructive testing.

With its focus on scientific-grade CCD imaging components and modules, SITe provides standard designs, user defined custom CCDs, and foundry services. SITe's engineering and manufacturing team builds custom CCD imagers for use in the most demanding applications, including NASA programs, satellite platforms, and other research projects. Devices are available as front illuminated or thinned, back illuminated CCDs.

Innovation, process development, and design experience date back to the founding of the group in 1974. For more information about scientific-grade CCDs, please contact SITe's customer service department.